Electronic Version

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Description

Reflective Arrayed Waveguide Grating

BACKGROUND OF INVENTION

[0001] *Field of Invention*

[0002] This invention relates to a photonic integrated circuit, specifically to a reflective arrayed waveguide grating, that is used for wavelength division multiplexing and demultiplexing for fiberoptic communication networks. It also relates to several other passive and active photonic device applications in the capacity of a building block via triple-phase integration described herein.

[0003] *Description of the Prior Art*

[0004] Recently arrayed waveguide gratings (AWGs) have proven to be an attractive vehicle for achieving high channel count wavelength division multiplexing (WDM) (see for example "An N×N optical multiplexer using a planar arrangement of two star couplers" disclosed by C. Dragone in IEEE Photonic Technology Letters, vol. 3, no. 9, 1991, pp 812815, or U.S. patent No. 0033715 A1 titled "Arrayed

waveguide grating having a reflective input coupling," Delisle, et al., Oct. 25, 2001). The basic strength and cost competitive success of this technology stems from the fact that it is built upon the strength of matured semiconductor fabrication (fab) technology. Many basic and precision fab facilities and advantages can be utilized in fabricating photonic integrated circuits (PICs) on silicon wafer or on other suitable wafers. The photonic components built on the surface of a wafer are generally known as the planar components; examples include planar waveguide, AWGs, interleavers, star couplers, variable optical attenuators (VOAs) and other integrated solutions that can be built around PIC chips. The planar star coupler, in fact, is the mother device for AWGs, because, in an AWG, two modified planar couplers are connected via an array of planar waveguides having a fixed path difference between successive ones, thereby acting as a grating. An analogy to the electronic ICs may be used to elucidate the photonic waveguides and PICs: PICs are the counterparts of the electronic ICs where photonic waveguides are the basic building blocks similar to the transistors for the ICs. Like transistors can perform switching, amplifying, and signal processing functions of electronic signal, photonic

waveguides and photonic integrated circuits can be designed to perform similar functions with light signals.

[0005] Detailed construction of a regular AWG is illustrated in Fig. 1, which for the ease of comparison, will be termed as a transmissive arrayed waveguide grating (TAWG) because it functions by transmitting light from the input through the device to the output. A TAWG is commonly used as a multiplexer (MUX) and/or a demultiplexer (DMUX). As shown in Fig. 1, a TAWG is built on a substrate *10* on which waveguides and slabs are fabricated whose functionalities are described in the following. A TAWG has the following main functional parts: a single or plurality of input waveguides *3*, an input slab *4*, an array of waveguides containing plurality of neighboring waveguides *5*, an output slab *6*, and a plurality of output waveguides *7* whose number typically equals to the number of channels of the device.

[0006] Referring to Fig. 1, the functionality of a TAWG can be briefly explained as follows. The input waveguide *3* carries a multiplexed signal to the input slab *4* that couples the signal to the array of waveguides *5*. The waveguides in the array are fabricated with a constant path difference, ΔL, between the neighbors. These waveguides lead the multi-

plexed signal to the output slab *6*. Because of the path difference between successive waveguides, the light undergoes interference; the intensity of constructive interference is focused at well-defined positions at the other end of the output slab *6A*. Here, output waveguides *7* are fabricated at calculated positions to collect the signals that are already separated into constituent wavelengths by the interference mechanism, thus completing the demultiplexing function. The multiplexing is achieved by following a reverse path: since the AWG works as a spectrograph device, when individual wavelengths (signals) are launched into the waveguides *7* attached to the output slab *6*, they will form a combined or "multiplexed" signal at the end of the input slab *4*. Thus a TAWG (e.g., the one shown in Fig. 1) functions by means of transmitting light from the input terminal via the input waveguide through the entire device.

[0007] The structure as a whole *11* referred to as an optical chip or a photonic integrated circuit (PIC), because it is constructed by assembling the waveguide elements in an integrated fashion. While in the current practice of PICs it is not implemented yet, this inventor envisions that a PIC may also contain additional elements such as modulator,

amplifier and detector on the same substrate, thus qualifying the PIC as a platform for designing many passive and active photonic devices via triple-phase integration, as described in the preferred embodiments.

[0008] The TAWG described above suffers from several disadvantages such as bigger area per device, longer waveguide lengths in the array, and two different slabs for input and output, all of which contribute to a higher insertion loss. Two different fiber-array interfaces are required for packaging; one for input and one for output. Having two different external interfaces is also disadvantageous, because, attaching two different fiber arrays increases the packaging loss, makes it relatively less reliable, and increases chance of failure.

[0009] *AWG Size Reduction*

[0010] A compact design of AWGs has been the subject matter of many contemporary investigations. Here we review available designs as published in the literature with a view to contrast the present invention with the previous attempts.

[0011] A design titled "Silica-based arrayed waveguide grating circuits as optical splitter/router," published in Electronics Letters, vol. 31, No. 9, 1995, pp 726—727, by Y. Inoue, A. Himeno, K. Moriwaki and M. Kawachi, proposed a reflec-

tion type arrayed waveguide grating circuit for optical power splitting and wavelength routing functions. The authors reported 1×14 optical power splitter with a mean insertion loss of 15.5 dB and the wavelength router's insertion loss ranged from 5.2 dB to 8.5 dB (a channel non-uniformity of 3.3 dB) with an inter-channel crosstalk of 19 dB.

[0012] Polarization insensitive, InP based DMUX was demonstrated for a 1×16 device [see "Small-size, polarization independent phased-array demultiplexers on InP," by H. Bissessur, B. Martin, R. Mestric and F. Gaborit, published in Electronics Letters, vol. 31, No. 24, 1995, pp 2118—2120] that exhibited an insertion loss of 8 dB and the crosstalk was 14 dB.

[0013] A design for two-slab waveguide grating routers via InP/InGaAsP material that would reduce the chip size was reported (see "Compact design waveguide grating routers," by T. Brenner, C. H. Joyner, and M. Zirngibl, published in Electronics Letters, vol. 32, no. 18, 1996, pp1660—1661). This design is based on a pair of interlaced conventional waveguide grating routers that share the slab area by means of a cleavage through the centers of the shared slabs (or free space region, in their nomenclature). The

reported on-chip transmission loss was 7.5 dB for the central channel and 1 dB higher for the outermost ports of the 8-channel device. The reported crosstalk was on the order of 20 dB.

[0014] InP based waveguide grating router's size reduction by folding back the input/output ports and exploiting mirror reflections off of multiple facets created by cleaves was reported (see "Size reduction of waveguide grating router through folding back the input/output fanouts," by M. Zirngibl, C. H. Joyner, and J. C. Centanni, published in Electronics Letters, vol. 33, No. 4, 1997, pp 295—297). They reported an insertion loss of 4 dB for the best channel measured against a straight test waveguide and 2-3 dB more for triple cleaved router. No crosstalk number was reported.

[0015] A reflective waveguide array demultiplexer using electro-optic $LiNbO_3$ was proposed (see "Reflective waveguide array demultiplexer in $LiNbO_3$," by H. Okayama, M. Kawahara, and T. Kamijoh, in Journal of Lightwave Technology, vol. 14, No. 6, 1996, pp 985—990). For a 1×4 device, the authors have reported an insertion loss of 15 dB and crosstalk ranging from 12 to 25 dB.

[0016] It is clear from the above review that previous attempts of

the chip's size reduction of several photonic integrated circuits have enjoyed a partial success. In all cases, however, size reduction is accompanied by a higher loss and lower performance. The present invention addresses the chip size reduction with simultaneous improvement of the device performance, and outlines methods of using the RAWG as a building block to fabricate additional devices via triple-phase integration.

SUMMARY OF INVENTION

[0017] This invention discloses a "reflective arrayed waveguide grating," (RAWG) for optical multiplexing and demultiplexing applications that uses a single slab for both input and output. It also uses shorter length of the waveguides in the array, thereby reducing the chip size to half compared to a TAWG. By eliminating one of the slabs, the design allows for a single external fiber array interface to the chip. These factors reduce the chip size and on-chip losses significantly. Moreover, the waveguide lengths are also half compared to what is necessary for a TAWG, thus contributing to lower insertion loss and significant savings of the silicon real estate. The smaller chip size increases the reliability of the device significantly and almost doubles the yield of chips per wafer. Used as a "building

block," these chips enable fabrication of several passive and active modules in an integrated platform.

BRIEF DESCRIPTION OF DRAWINGS

[0018] Fig. 1 shows a two-slab transmissive arrayed waveguide grating (TAWG) (prior art) and its constituent parts.

[0019] Fig. 2a shows the spectral response of the device shown in Fig. 1, and 2b shows a plot of the insertion loss of all channels.

[0020] Fig. 3 shows the construction of a reflective arrayed waveguide grating (preferred art) along with its constituent parts.

[0021] Fig. 4 is a sketch of the reflective mirror.

[0022] Fig. 5 is an alternative embodiment of the preferred art.

[0023] Fig. 6 shows the spectral response of an eight-channel RAWG.

[0024] Fig. 7 shows the spectral response of a 16-channel RAWG.

[0025] Fig. 8 exhibits the spectral response of a 48-channel TAWG.

[0026] Fig. 9 shows the insertion loss of the RAWG as extracted from Fig. 6.

[0027] Fig. 10 shows the insertion loss of a 16 channel RAWG as extracted from Fig. 7.

[0028] Fig. 11 shows the insertion loss of a 48 channel TAWG as extracted from Fig. 8.

[0029] Fig. 12 shows the details of waveguide construction.

[0030] Fig. 13 is an example of a second-phase integration of a PIC with an amplifier block constructed monolithically on a substrate. The PIC is connected to the amplifier via waveguide interconnect.

[0031] Fig. 14 is an example of a third-phase integration of a PIC with a modulator block and amplifier block constructed monolithically on a substrate. All components are inter-connected via on-chip waveguide interconnects.

Preferred Embodiment

[0032] The current invention describes a solution to the size reduction problem with a goal to reduce the chip size with simultaneous improvement of performance in terms of reduced loss and external interface. The most compelling rationale for size reduction are: (i) yield per wafer will increase as the size per chip is reduced; this in turn will cut the cost of the devices, (ii) smaller chip size will result in smaller package size, and (iii) it is easier to maintain temperature uniformity of a smaller chip and smaller package which is crucial for reliable device operation.

[0033] In addition to the size reduction, other objectives of the present invention are to reduce the on-chip loss and also to reduce the external interfaces to improve the reliability of the devices built around this chip. The device disclosed herein accomplishes all three objectives. A further objective is to use these chips as a building block for triple-phase integration.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

[0034] The preferred art is described by the illustrations in Fig. 3 through Fig. 6. Fig. 3 is a schematic view showing a first embodiment of the "reflective arrayed waveguide grating" (RAWG). Referring to Fig. 3, the preferred art is composed of a plurality of waveguides *22*, a slab *23*, an array of waveguides *24*, and a reflective surface or mirror *26* (Fig. 4); all of which is fabricated on a substrate *30*. The whole assembly is referred to as a photonic integrated circuit (PIC) or alternatively an optical chip *25*.

[0035] There are n waveguides, numbered *21.1...21.n*, connected to the input end *23a* of the slab *23*. These waveguides can serve as both input and output; as such any of these waveguides can be used to launch an input signal into the device. For illustration purposes, Fig.3 shows that a multiplexed input signal composed of n-wavelengths is

launched into the waveguide *21.1*. The remaining waveguides, *21.2...21.n* serve as output channels for the demultiplexing function of the device. Similarly, the input signal can be launched into any of the waveguides while all other waveguides (except the input) will automatically function as output waveguides. For multiplexing functions, n-1 wavelengths can be launched into consecutive n-1 waveguides such as *21.2...21.n*. These signals will then combine together and be focused into waveguide *21.1*, thereby completing multiplexing function.

[0036] An input multiplexed signal composed of a plurality of wavelengths, $\lambda_1 + \lambda_2 + \ldots + \lambda_n$, launched into an input waveguide, say *21.1*, will travel through the input waveguide and then shine into the slab *23a* in the form of a cone whose spread will cover all waveguides in the array *24* meeting the other end of the slab *23b* thereby the signal will get coupled to the array of waveguides *24*. The multiplexed signal will travel through the waveguides and then be reflected back by the mirror *26* that terminates the waveguides. This reflected signal undergoes a total roundtrip path difference of ΔL between successive waveguides. Because of this path difference, light of different wavelength undergoes constructive and destructive

interference, thereby separating the multiplexed signal into constituent wavelengths. The intensity of constructive interference is composed of demultiplexed wavelengths that are focused on the waveguides *21.2...21.n* at the slab interface. Thus, waveguides *21.2...21.n* serve as the output channels, completing the demultiplexing function.

[0037] Multiplexing is accomplished by following a reverse path. Individual wavelengths launched in n-1 waveguides, e.g., *21.2...21.n* will travel through the slab and the array of waveguides, then will be reflected back at the mirror *26* and the combined wavelengths will be focused at the position where waveguide *21.1* will carry the signal to output fiber.

[0038] Fig. 5 shows an alternate preferred embodiment of the reflective arrayed waveguide grating. Here waveguides *41.1...41.n* serve identical functions as *21.1...21.n* described above in reference to Fig. 3, except their construction is such that it helps further reduction of the chip size. Similarly, items *42*, *43*, and *44* perform identical functions as items *22*, *23*, and *24*, as described in the foregoing paragraphs in reference to Fig. 3.

[0039] The fabrication specifics of the waveguides are described in the next section. Following the principle described

above, RAWGs can be designed for any number of channels such as 4, 8, 12, 16, 24, 32, 48, etc. Here we have given examples of an eight channel, a sixteen channel and a forty-eight channel device. The example of 48-channel device is described in terms of a TAWG here; however, it can be constructed as a RAWG as well.

[0040] Additionally channel spacing of a given RAWG can be designed to comply with ITU-T definitions such as 0.25 nm (~31 GHz), 0.4 nm (50 GHz), 0.8 nm (100 GHz), 1.6 nm (200 GHz), 4 nm (500 GHz), and so on, and individual channel frequencies can be designed to match the ITU grid frequencies.

[0041] Fig. 6 shows the spectral response of a RAWG that was constructed as an 8-channel device. Fig. 7 shows the spectral response of a RAWG designed for 16-channel and Fig. 8 shows the spectral response of a 48-channel TAWG. The design parameters for these devices are listed in Table 1. Fig. 9 shows the insertion loss of all channels of the 8-channel RAWG corresponding to the spectra in Fig. 6. The insertion loss of a 16-channel RAWG is shown in Fig. 10 (extracted from the spectral response of Fig. 7) and the insertion loss of a 48-channel TAWG are shown in Fig. 11 as extracted from the spectral response of Fig. 8.

[0042]

Table 1. Critical design parameters for the RAWGs and the TAWGs whose spectra are shown in Figs. 2a, 6, 7, and 8.				
Parameter (Unit)	**8-channel RAWG**	**16-channel RAWG**	**48-channel TAWG**	**8-channel TAWG**
Number of I/O waveguides	9	17	1 input 48 output	1 input 8 output
Slab length (μm)	3700	6900	19300	4100
Slab width (μm)	1850	3450	9650	2050
Waveguide width (μm)	6	6	6	6
Number of waveguide in the array	37	69	193	41
Path difference, ΔL (μm)	150	128	128	128
Center channel loss insertion (dB)	2.53	2.84	6.18	5.40

[0043] *Construction of the waveguides and fabrication of the chip*

[0044] Optical waveguides are conveniently constructed on a suitable substrate such as a silicon wafer by fabricating the core and the cladding in separate steps. An example is exhibited in Fig. 12 which shows a cross-sectional view of a waveguide construction.

[0045] A silicon (Si) wafer *100* is used as a substrate on which a layer of film *101* can be formed via a method that is common knowledge to people expert in this art, such as, spin-coating. The Si substrate has a refractive index in the range 3.4 and 3.5 and the first layer *101* can be formed from a material such as silica or a polymer (e.g., dendrimer) having a typical refractive index in the range 1.45 and 1.47. This layer *101* with a typical thickness 5—6 μm

becomes part of the cladding. Another layer *103* is then deposited on top of the previous layer from a material such as doped silica or dendrimer having slightly higher refractive index than the first layer *101*. This layer *103* will form the core of the waveguide and the material for this layer can be either silica or polymeric; the only requirement is that its refractive index should be higher than the cladding layer. This layer's typical thickness can also be 5—6 μm, depending on the design. A typical value for refractive index contrast between the cladding and the core layer is of the order of 0.5—2%.

[0046] The layer *103* is then patterned by defining square ridges to form the core of the waveguide. The patterning can be done by an etching process such as reactive ion etching (RIE), or wet etching, or by e-beam lithography, depending on the material used to form the layer. The goal of etching is to form sharp walled ridges that form the waveguide core *103*. Prior to etching, a mask is laid on the layer. For the RIE process, the mask allows the areas that will form the ridges to be protected while the exposed areas are removed. Only one core is shown in Fig. 12, however, plurality of cores can be formed from the same mask whose number depends on design and application; each

core forms an independent waveguide after cladding layers are deposited. For instance, for an eight channel RAWG, as many as 35—50 waveguides may be necessary (depending on a given design). Core dimension also depends on a given design; typical dimension is 6×6 μm^2 as used in the example of Fig. 3. For this design 37 waveguides were constructed in the array *24* where the constant path difference between neighboring waveguides in the array is 150 μm.

[0047] After the etching process is completed, the entire surface is coated with another layer *102* from the same material and having identical refractive index as layer *101*, to fill-in the intra-ridge spaces created by the removal of material during etching. This layer is further grown by depositing more of the same material by spin coating to form the cladding layer *104*. The end result is the core *103* is completely covered by the cladding layers *101*, *102* and *104*. Finally a layer of film is deposited on the entire surface from a common material such as poly siloxane. This layer *105* serves as a cover layer to protect the waveguide structure, and its refractive index is not specified.

[0048] The slab *23* is also constructed by the same layer by layer approach described above. In practical fabrication pro-

cess, the whole structure, i.e., the waveguides and the slab, all are constructed simultaneously from a single mask. The slab dimensions of the example in Fig. 3 is 3700 μm length (center *23a* to center *23b* of the arches), 1850 μm width, and a thickness of 6 μm. (See table 1 for other dimensions).

[0049] The mirror *26* has a length of 3735 μm and a thickness w of approximately 10 μm (see Fig. 4). The width of the mirror is the same as the thickness of the chip; it can be produced by evaporating a layer of gold or any other high reflectivity metal on the side of the chip with an appropriate mask. The mirror length will also depend on a given design, usually longer for higher channel device.

[0050] *Triple-phase Integration*

[0051] While tiers of integration has been used in many electronic ICs such as in application specific ICs (ASICs) or multi-module ICs (MMICs), these integrations are mostly hybrid. That is separate ICs are packaged together to meet the need of specific applications. Some hybrid integration has also been attempted for PICs. However, the ability of a monolithic integration of multiple photonic functionalities on a single substrate has a great potential for system simplification, cost-effectiveness, and performance enhance-

ment. Such a scale of integration can be achieved by integrating the PIC described herein over three main tiers, a scheme termed as "triple-phase integration."

[0052] At the first phase of integration in the passive domain, the PIC can be used to design a number of photonic devices such as multi-channel tunable optical add/drop multiplexer, multi-channel variable optical attenuator, multi-channel optical channel monitor, multi-channel tunable optical gain equalizer, multi-channel thermo-optic switch, interleavers, etc.

[0053] At the second phase of integration, these chips can be combined with appropriate on-chip gain medium (e.g., Er^{3+} doped waveguide) to produce the above mentioned PICs with extremely low-loss and/or with a gain. This is important, because, current optical transmission systems require frequent signal amplification and regeneration (also called repeater) which is expensive. Ability to build systems with extremely low-loss and/or gain will simplify system design significantly. It will also eliminate the frequent need of repeaters, thus enabling significant cost reduction and ease of deployment.

[0054] The third phase of integration will allow combining these low-loss PICs with active elements such as laser-diodes or

VCSELS, detector arrays, and electro-optic modulators to produce a line of optronic modules and systems. Examples include, multi-channel modulators, receivers, transmitters, transceivers and transponders, and fully built out DWDM systems.

[0055] *Example of Triple-phase Integration*

[0056] Some examples of first-phase, second-phase and third-phase integration are included. The RAWG itself (e.g., Fig. 3) is an example of first-phase integration of waveguide elements such as ridge and slab waveguides. Other examples of first-phase integration include optical power splitter, interleaver, and combination of interleaver and RAWG based PICs.

[0057] Fig. 13 shows an example of a second-phase chip-scale integration of a PIC (specifically a RAWG) with an amplifier block constructed monolithically on a substrate. Here a passive device (the RAWG) is integrated with an active unit (the amplifier) by monolithic way (i.e., fabricated on the same substrate). The PIC is connected to the amplifier via waveguide interconnect. The RAWG, the amplifier block, and the waveguide interconnects, all fabricated by a layer by layer approach as described in connection with Fig. 12. Optical amplifiers are pumped by an external laser to pro-

duce amplification. That is, the amplifying material such as Erbium doped dendrimer or glass absorbs light in the 890 nm and 1480 nm regions, and emits light in the 1310 nm and 1550 nm regions. This additional emission in the 1550 nm region (or in the 1310 nm regions) strengthens the input signal by increasing its intensity. Usually a WDM coupler is used to combine the pump laser and optical signal at the input of the amplifier and another WDM coupler is used to separate the pump from amplified signal at the output. In the scheme shown in Fig. 13, the chip can be used as a self-contained unit via the second-phase integration where no external WDM coupler is necessary. The waveguide interconnect can be used for coupling the pump laser and input signal into the amplifier block. Also by using the spectrograph properties of the RAWG, this scheme can eliminate the need of a WDM coupler at the output end as well. Thus the second-phase integration is advantageous because it can eliminate attaching external WDM couplers and thus can enable a true chip-scale PIC; the assembly is termed as an amplified PIC (APIC).

[0058] Fig. 14 is an example of a third-phase chip-scale integration of a PIC with a modulator and amplifier block constructed monolithically on a substrate. Here three differ-

ent components are integrated: a RAWG (passive unit), an amplifier (active unit), and a modulator (a signal processing unit). All components are interconnected via on-chip waveguide. The RAWG, the modulator block, and the amplifier block, all can be fabricated from a single mask via a layer by layer approach as described in connection with Fig. 12; the assembly is termed as an amplified electronic PIC (AEPIC). In addition, active elements such as laser diodes, VCSELs, and detectors can also be fabricated on the same substrate using separate masks and material. Such an assembly, if constructed without an amplifier block, may be termed as an electronic PIC (EPIC). Many active elements such as laser diodes and modulators require metallization for electrodes attachment; this can be done using a separate mask via metal evaporation or sputtering process.